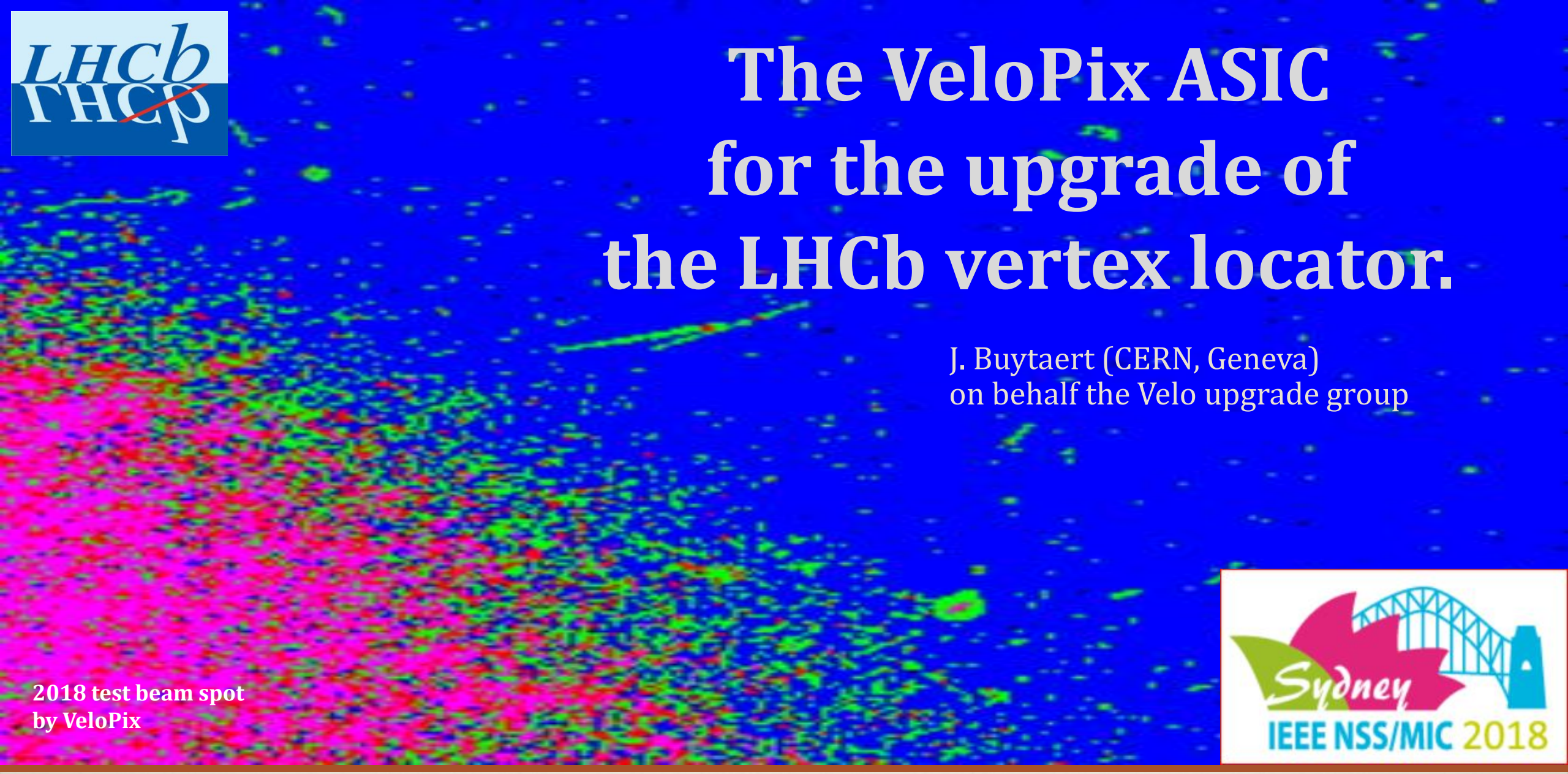
The VeloPix ASIC for the upgrade of the LHCb vertex locator.

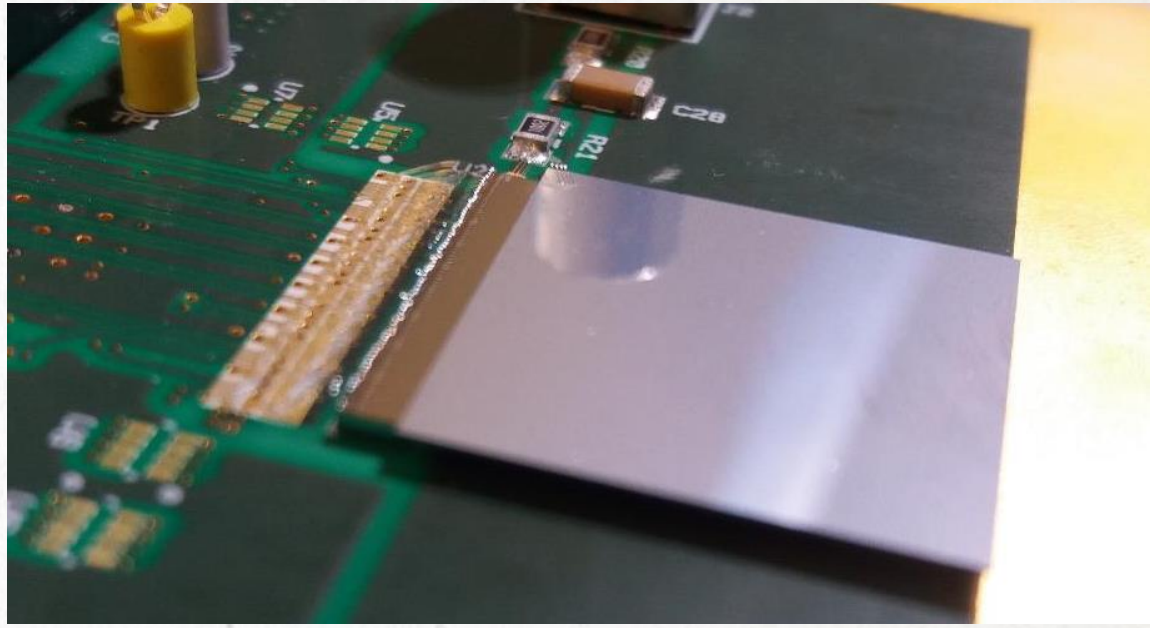
J. Buytaert (CERN, Geneva)
on behalf the Velo upgrade group



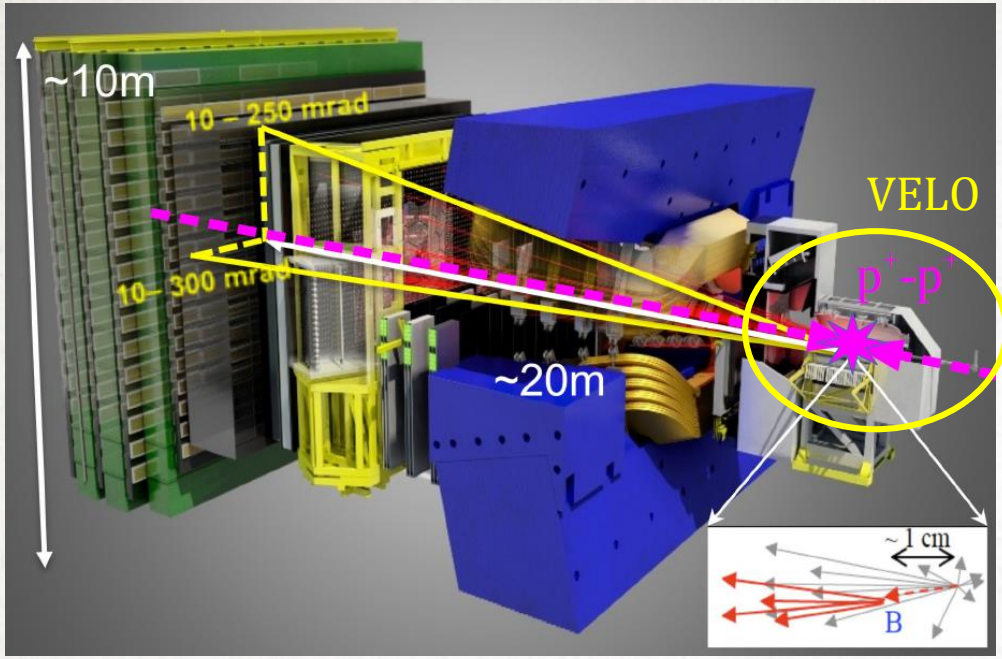
2018 test beam spot
by VeloPix

Contents:

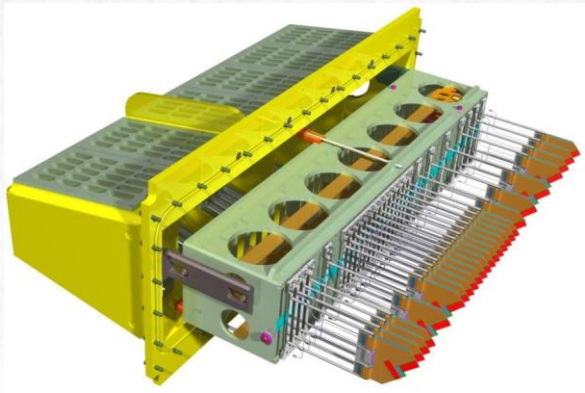
- Context of LHCb Velo upgrade.
- Overview of the VeloPix ASIC.
- Analogue & digital functionality of pixel cell.
- Internal data readout path.
- Radiation qualification.
- Production of ASIC.
- Summary.



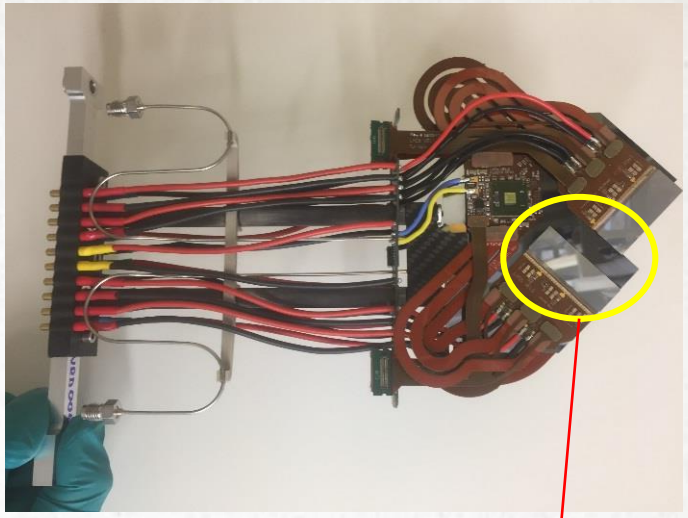
LHCb VELO upgrade.



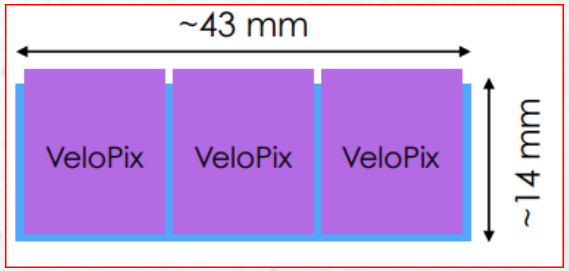
VELO detector:
2 x 26 modules



VELO module.



Pixel sensor bump bonded to 3 VeloPix ASICs .



- LHCb is a dedicated experiment at CERN's LHC searching for **new physics** by studying **CP violation** and rare decays of b and c quarks.
- Forward angle spectrometer with **excellent vertex resolution** and PID
- A full detector upgrade will be installed in **2019-2020** to reach **5x higher luminosity** and **improved efficiency**.
- No more hardware trigger → all **data is read out @40MHz** and sent to a CPU farm.

Poster N-22-152 –
"The LHCb Upgrade Program"
(Wednesday, 14, 10:20 AM)

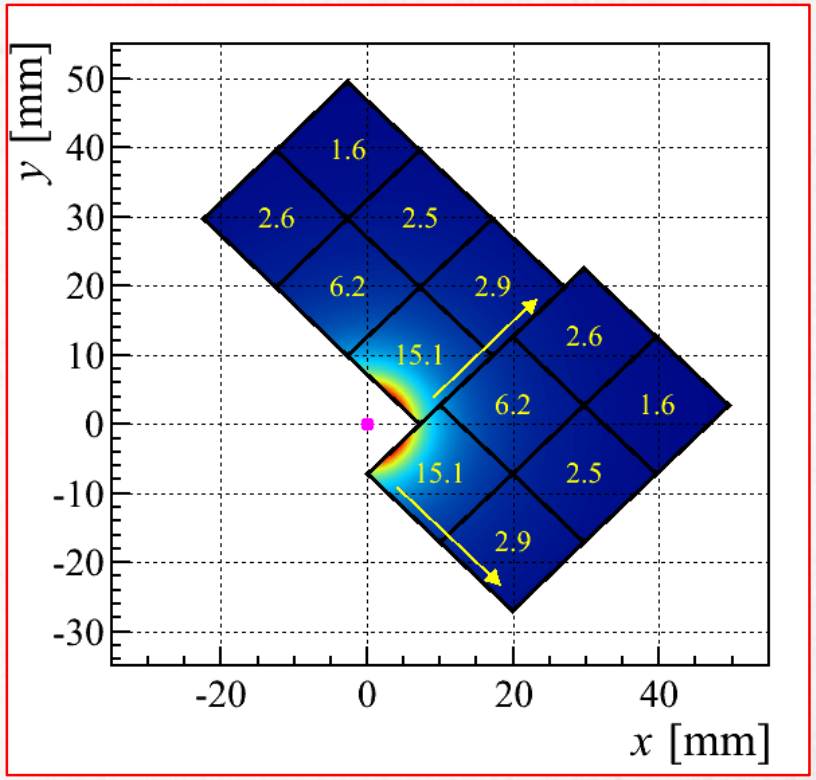
N-26-01 –
"The LHCb VELO Upgrade"
(Wednesday, 14, 1:40 PM)

N-32-01 – The Timepix3 Telescope and Sensor R&D for the LHCb VELO Upgrade
(Thursday, 15, 8:00 AM)

Requirements for VeloPix.

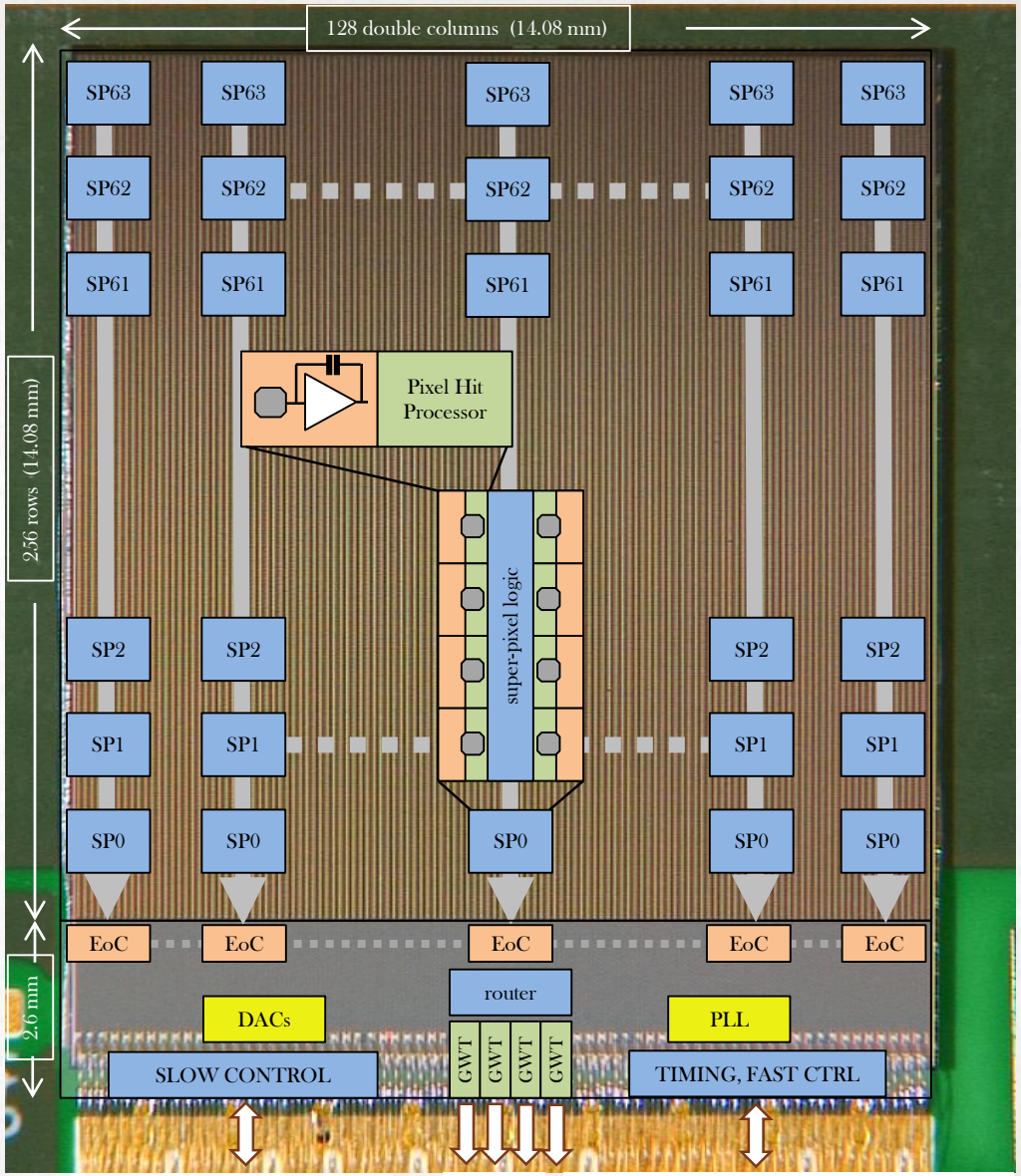
- Sustain readout of **600 million particles/s** for the hottest ASIC : > **15 Gbit/s**
- With a hit detection **efficiency > 99%** at highest occupancy region.
  - **fast return to baseline** (16 ke^- in ~300 ns)
  - operational **threshold at ≤ 1 ke-** (expected signal from sensor at end of life ~7ke^-)
- SEE & TID **radiation hardness** to
  - 400 Mrad and 8 x 10^15 1MeVn_{eq}/cm^2 (non-uniform particle fluence)
  - Capable of 12 nA pixel leakage current.
- Power consumption < 3 W

Data rates per ASIC (Gbit/s)

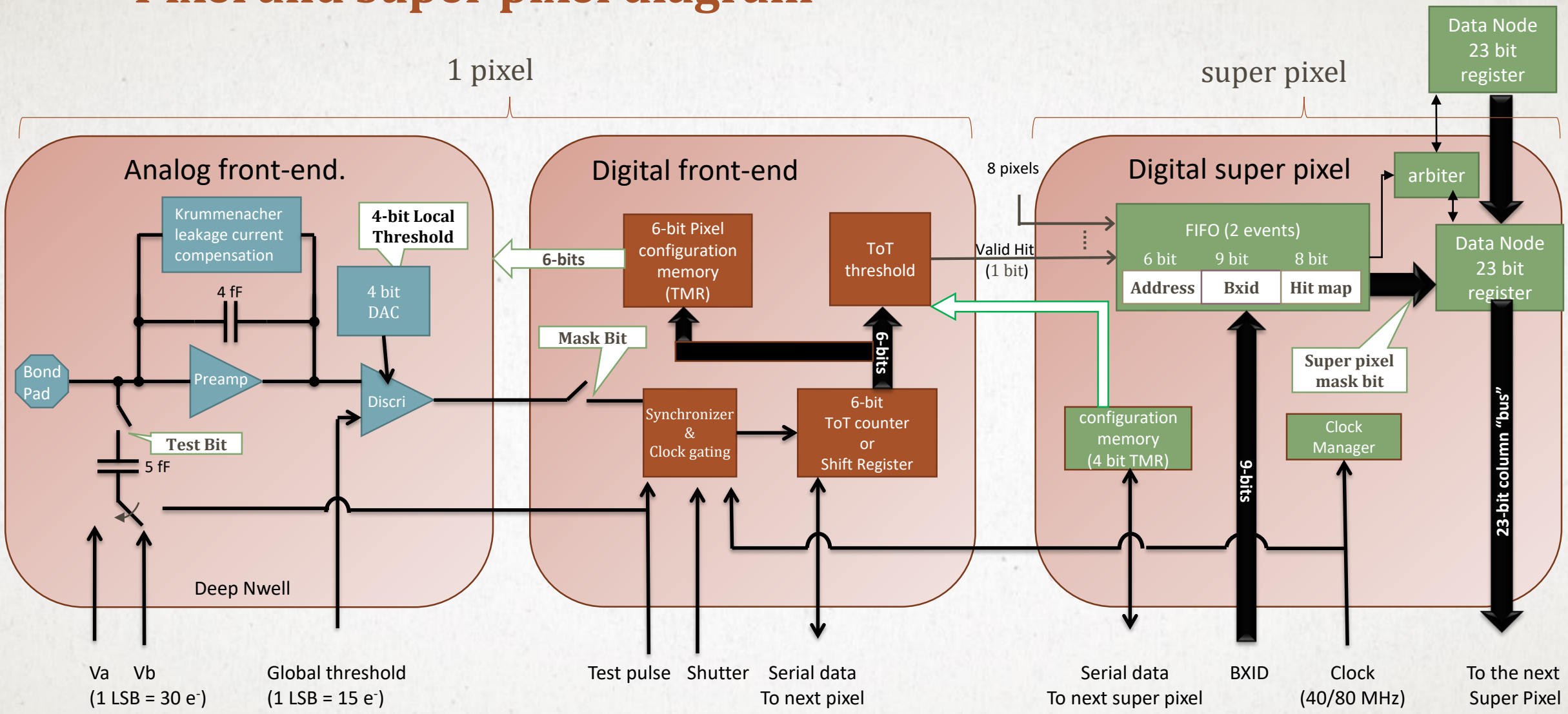


VeloPix overview

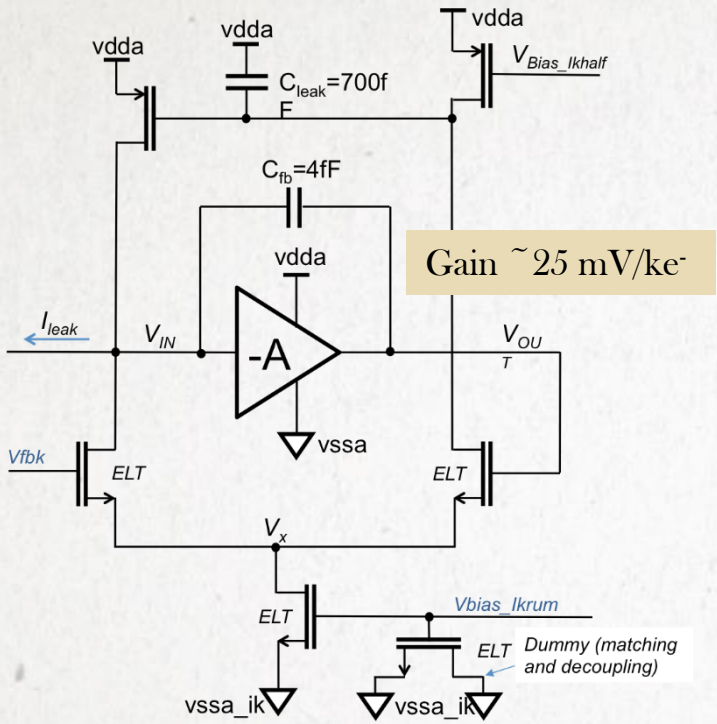
- Array of 256 x 256 pixels (55 x 55 μm^2).
- optimized for **e$^-$ collection** (n-in-p sensors)
- Data readout:
  - Capable of 800 M pixelhit/s for full ASIC.
  - **Trigger-less, data driven**.
  - All data directed to a **central crossbar router**.
  - 4 high speed **5.12 Gbit/s serial outputs** "GWT".
- "**Super-pixel**" blocks:
  - 8 pixels share common digital functionality.
  - 30% reduction of data volume.
- Primary readout is **binary** pixel hit.
  - a special readout mode allows to read **charge amplitude**.
- Implemented in **130 nm CMOS** using a custom CERN High density library for logic in pixel matrix.
- Power consumption ~1.5 W.



Pixel and super pixel diagram

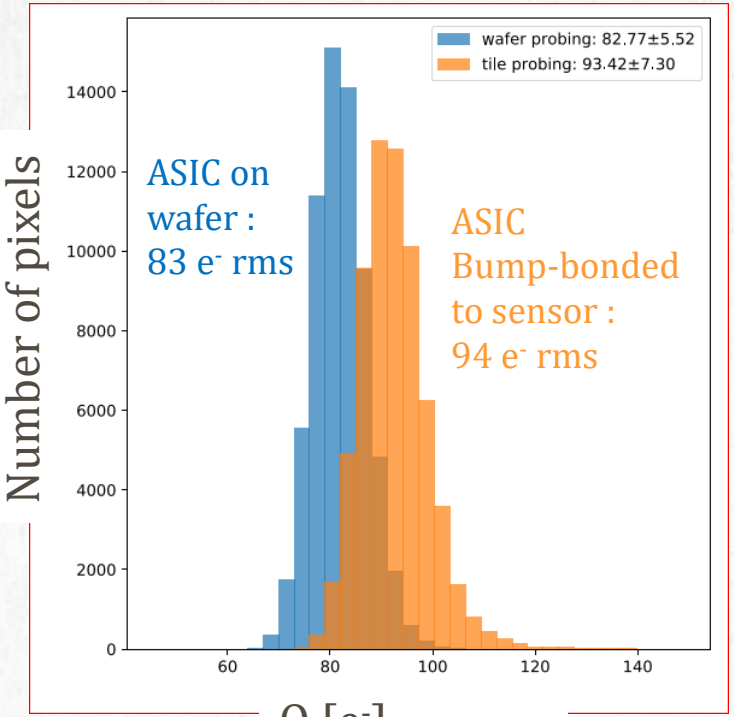


Pixel pre-amplifier.

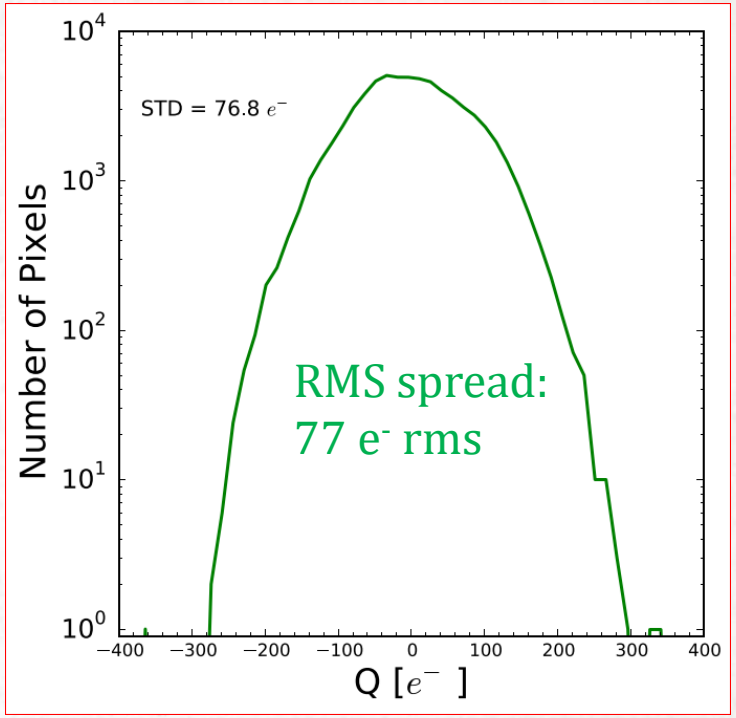


- Krummenacher feedback for leakage current compensation.
- Optimised for electron collection (n-in-p sensor)
- Power consumption ~2.5 μA/pixel .

Measured noise



Measured threshold spread after equalisation.

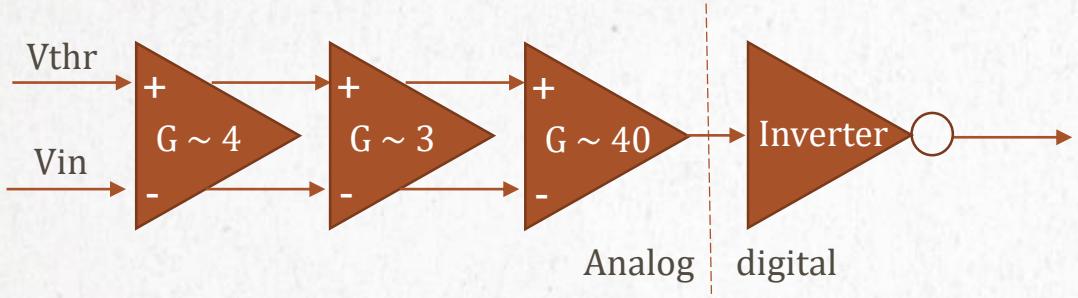


Expected operational threshold @ 6 x ENC_{total} ~ 726 e-

(ENC_{total} = ENC_{noise} ⊕ $ENC_{threshold}$ ~ 121 e-)

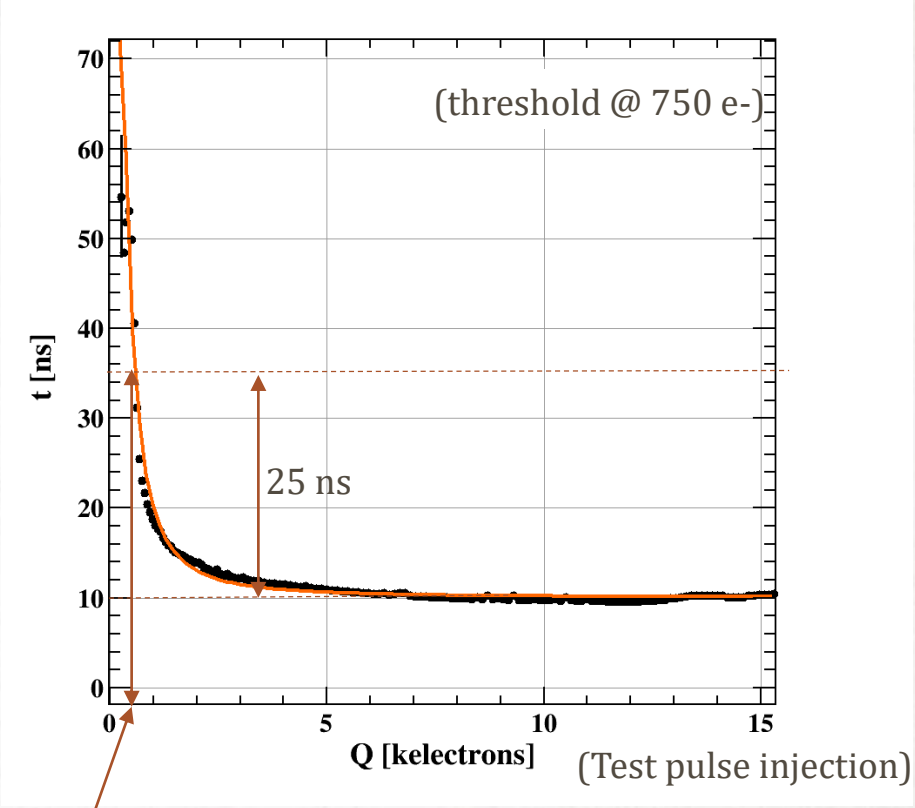
Pixel discriminator.

- Designed for **minimal time walk**.
  - Cascade of 3 differential amplifier stages.
  - 2 low gain stages & 1 high gain stage.



- Power consumption ~3.6 µA /pixel.

Measured time-walk

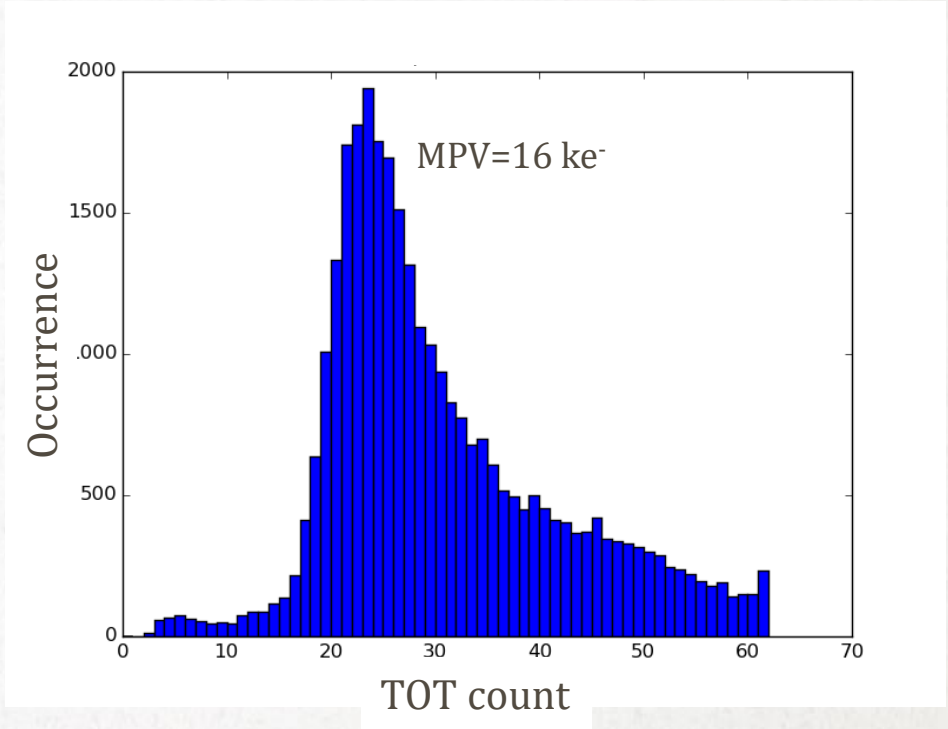


Minimal in-time charge = ~400 e^-

Pixel digital front-end

- The logic is **reconfigurable** as:
  - a **shift register**
    - for write/read to local pixel configuration memory .
  - a **TOT counter** (6bit):
    - acts as a “digital threshold” in normal readout: discriminator hits are accepted if ToT counter > 0,1,2,3 (programmable).
    - The counted value can be read through slow control interface (80Mbit/s). Used for monitoring charge collection from irradiated sensors.
  - A **hit counter** (6 bit) :
    - used during threshold equalisation procedure.

TOT readout of MIP charge collection in 200um Si sensor.



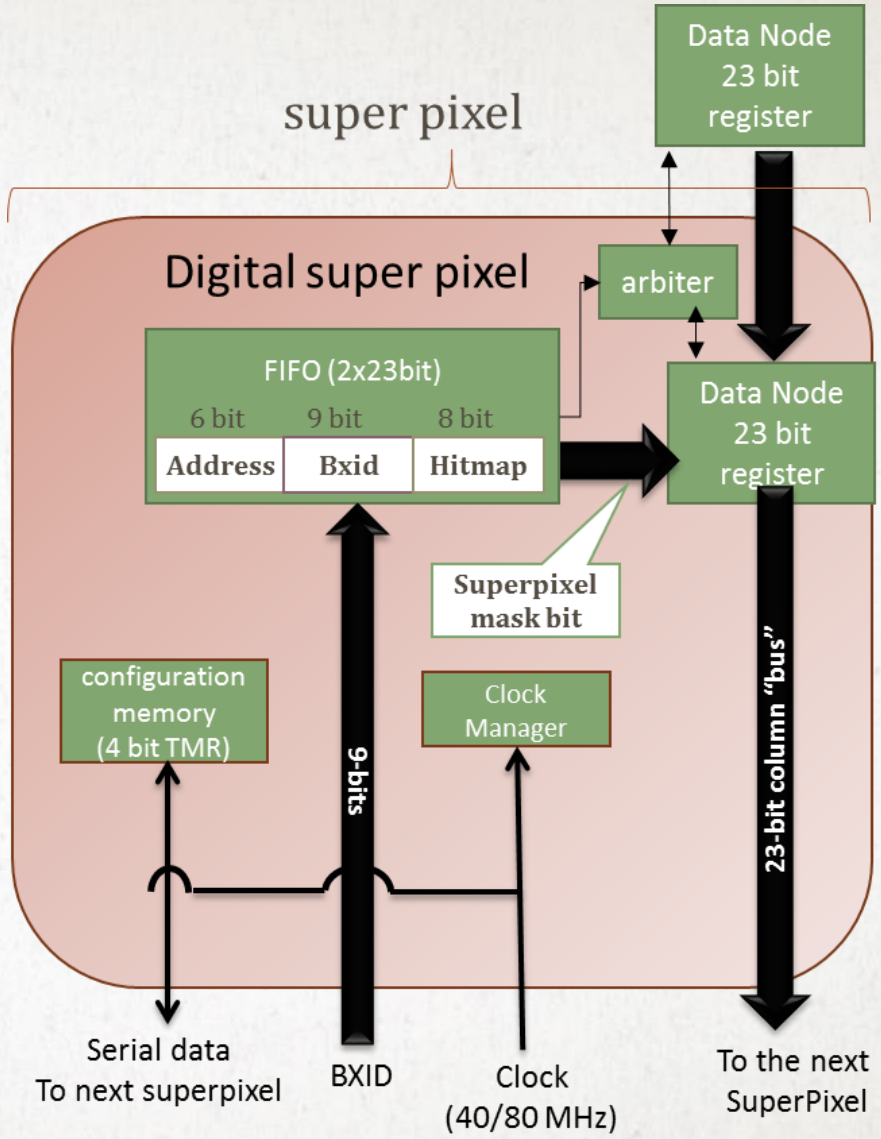
Super pixel

- It contains **common logic for 8 pixels**:
  - Common **FIFO buffer** (2 event deep buffer)
  - Common **address & time stamping**:
    - saves 30% in total data volume !
  - Common **data access to column bus**.
    - Arbiter provides fair sharing of column bus bandwidth.
  - **Data format** (23 bit) of Super Pixel Packet "SPP":

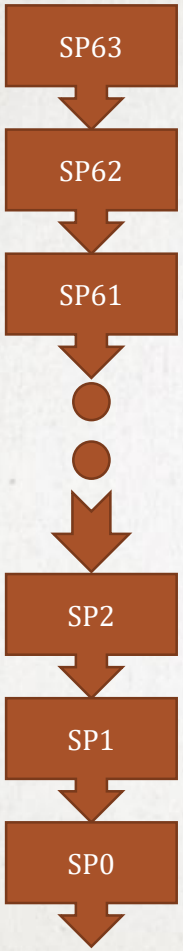
SP address 13b	Bxid 9b	Hit map 8b

- SEU protection :
  - Full triple redundancy implemented for FSM & configuration registers.
  - No protection for data registers. Low SEU can be tolerated.

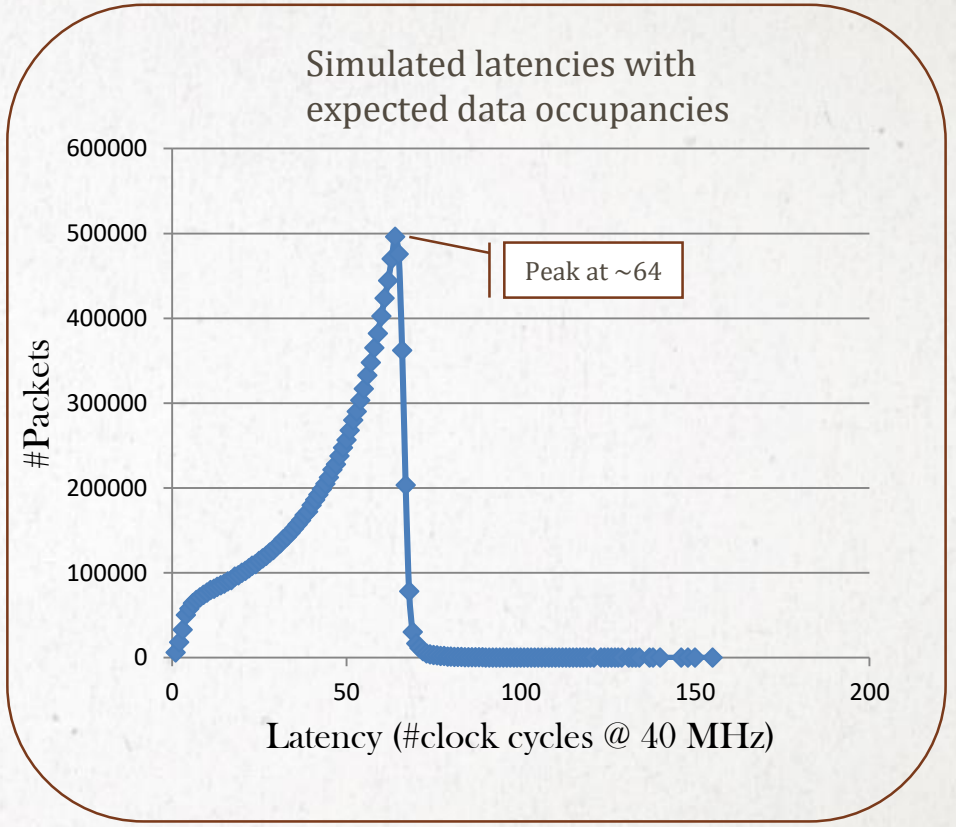
- All logic in pixel & super pixel is synthesized and auto-P&R



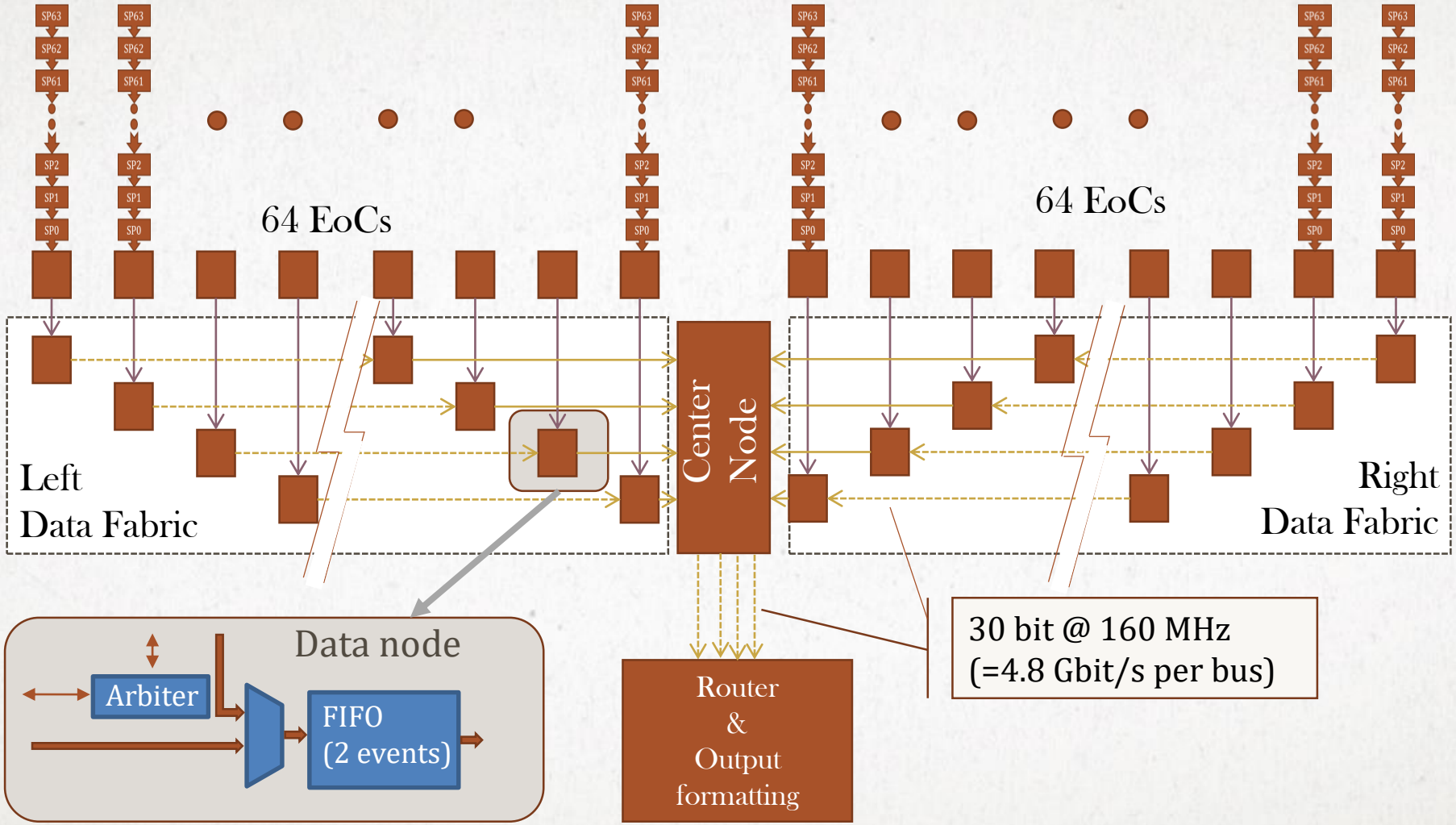
Internal readout : column «bus»



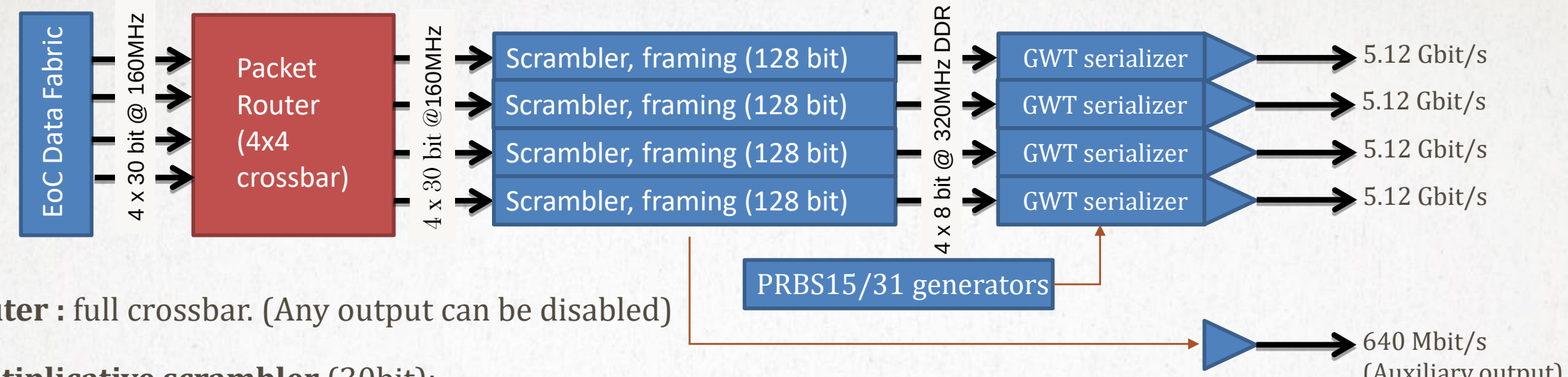
- «bus» = **cascade of 64 data nodes**.
  - data is transferred between nodes at each clock cycle.
  - More **power efficient & less time critical** than a standard bus with data transfers in single clock cycle (14mm long!).
- longer **latency** :
  - 64 clock cycles for transfer of SPP from top to bottom.
  - Latency is **not critical** for a trigger less data-driven acquisition.
  - latency must be ≤ 512 for **non-ambiguous time stamp**. (9 bit BCID)
- Maximum **data transfer rate** is 13.3 M packets/s.
  - handshake protocol between SP.
- **Arbitration** rule:
  - to guarantee fair sharing of bus bandwidth between all SP.



Internal readout : EOC «data fabric»



Internal readout : Router & Output formatting



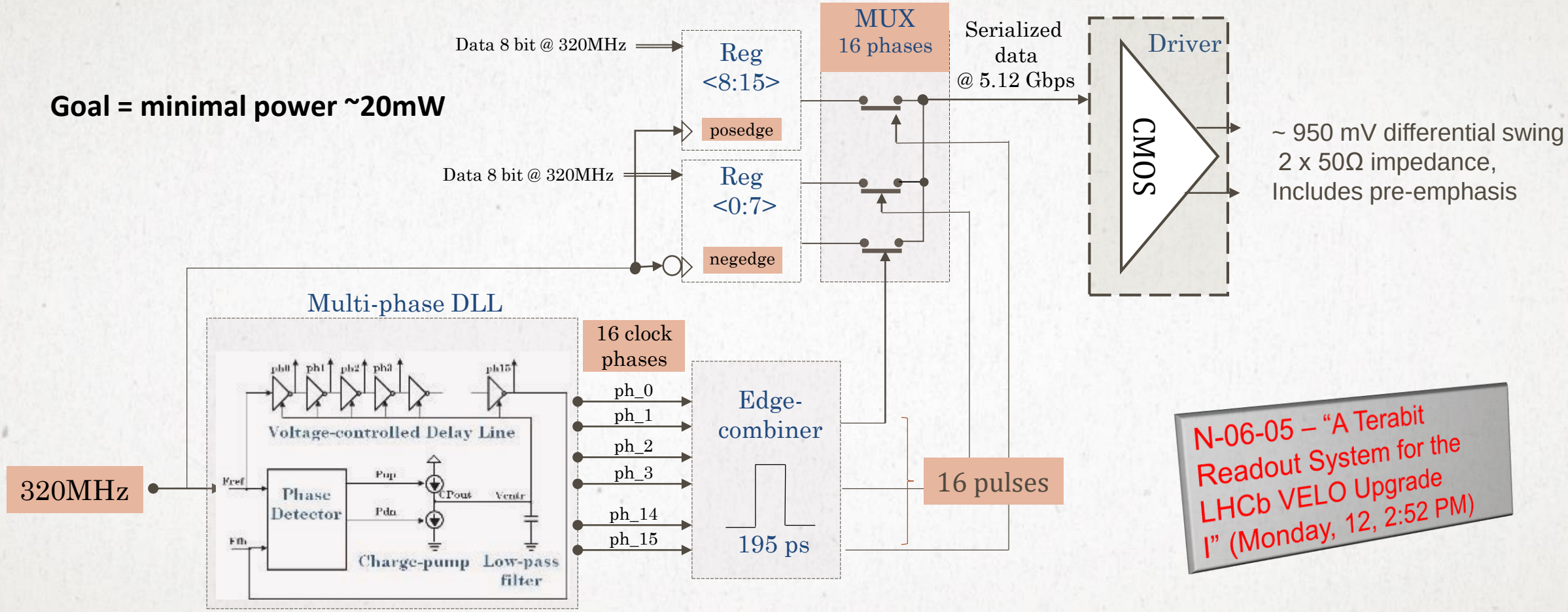
- **Router :** full crossbar. (Any output can be disabled)
- **Multiplicative scrambler** (30bit):
  - Line encoding for DC balance and clock recovery.
  - Self synchronising (no need for reset, seed or sync pattern). Decoding of 30 bit frame only depends on previous frame.
  - Limited propagation of bit transmission error: only loss of 2 frames of 30 bit.

GWT data frame format :

Header = 4b identifier + 4bit parity

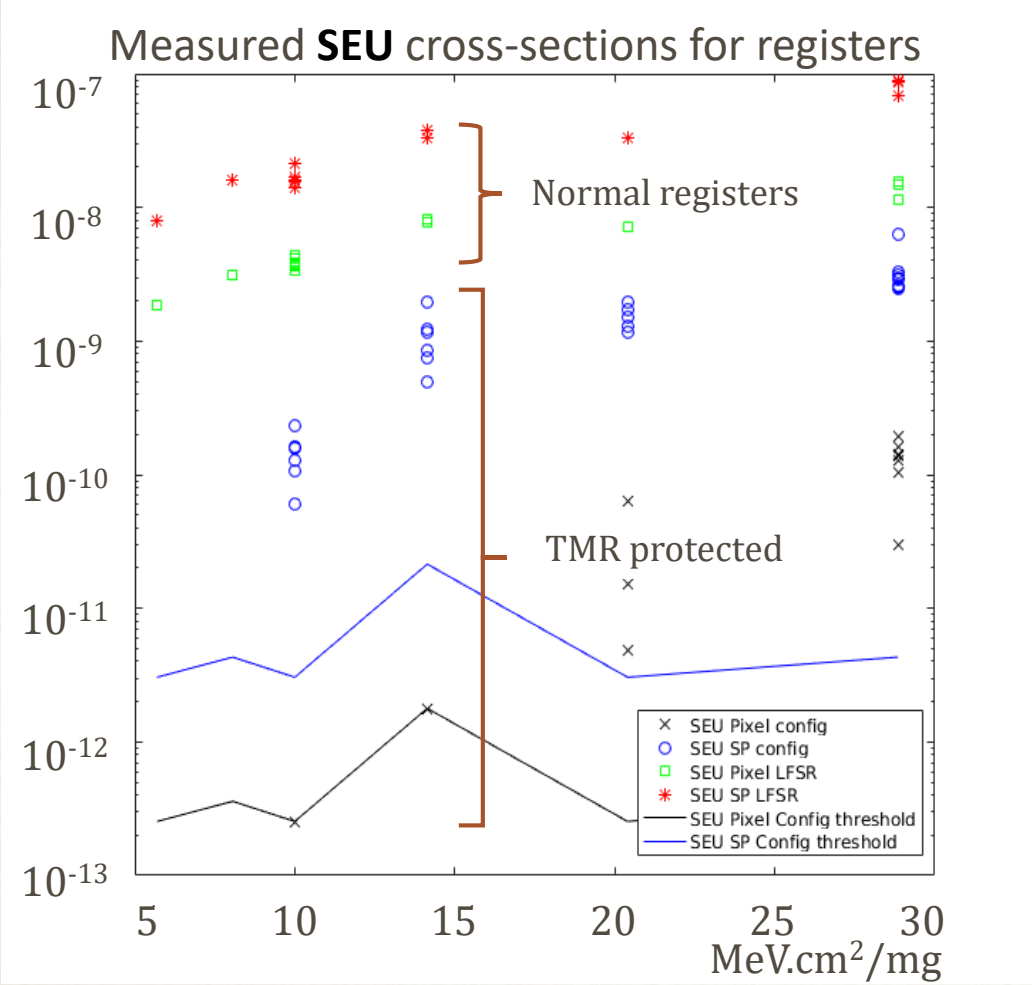
Internal readout : "GWT" Gigabit Wireline Transmitter

Goal = minimal power ~20mW



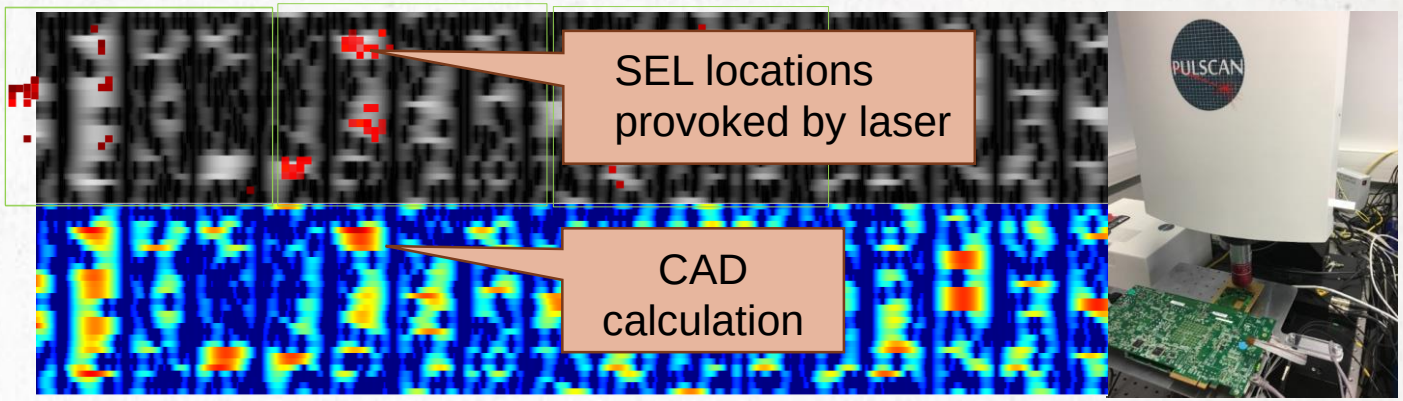
N-06-05 – "A Terabit Readout System for the LHCb VELO Upgrade I" (Monday, 12, 2:52 PM)

Radiation tests: SEU, SEL and TID.



Done at HIF (Heavy Ion Facility @ Louvain, BE)

Also observed **SEL** ("single event latch-ups"). First observation in 130 nm. Reason well understood and corrected. Predictions in CAD tool agree very well with micro-laser test (@facility in Montpellier, FR).



Total ionising dose was tested up to 400 Mrad with Xray:

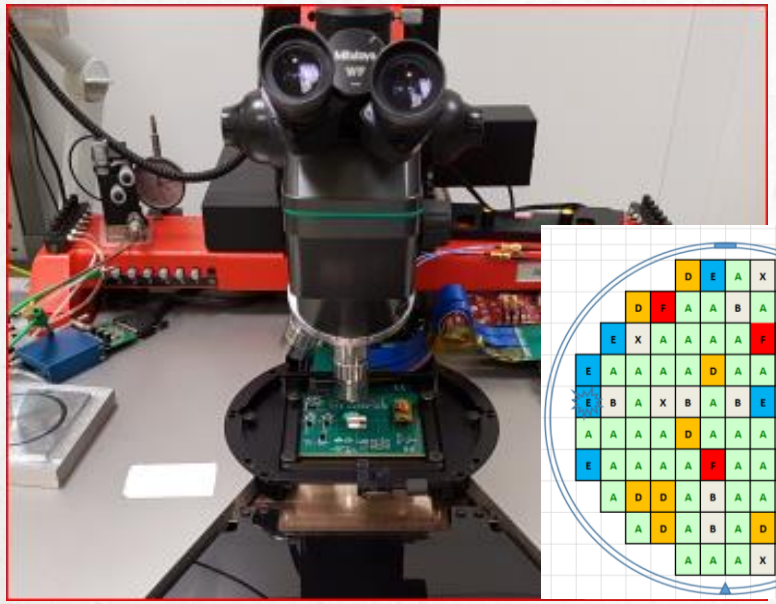
-No change in digital power consumption observed.

-No drift in analogue parameters (pixel thresholds & noise).

-Global DACs remain stable.

Production

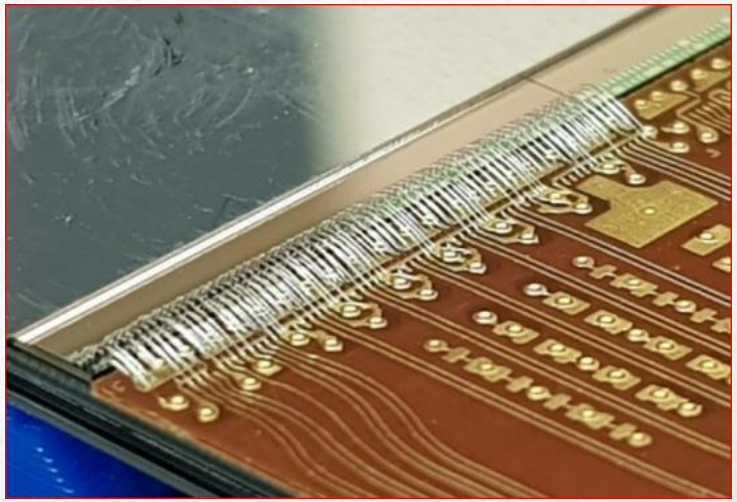
- **Wafer probe testing**:
  - 92 ASICs per wafer.
  - 1 wafer tested per day.
  - Yield is ~60% (on 12 wafers)



ASICs are retested after **bump bonding** to sensors. Verify bond connections : measured failure < 10^{-6}

First I/V measurement of sensors (biased up to 1000V in vacuum).

ASICs are **wire-bonded** to hybrids. I/O pad-layout was optimised during ASIC design.



Summary

- The VeloPix ASIC meets the challenging requirements of low-noise, high data readout speed and high radiation hardness.
- The ASICs have been produced & tested and first modules are being assembled.
- The new LHCb VELO pixel detector will be installed in 2019-2020.